Through Glass Vias (TGV) and Aspects of Reliability

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Abstract

Glass as a substrate for electronics packaging has many potential benefits, including the ability to tailor the thermomechanical and electrical properties of the glass to meet the demands of a given application. Because this process may entail modifications to the chemical composition of the glass, the impact of the composition changes to the long term reliability of the electronic package should be carefully considered. Here, two different compositions of glass are examined with regards to their use as a glass interposer, and specific aspects of their reliability are tested. A glass interposer design was fabricated on glass substrates of two different coefficients of thermal expansion (CTEs), 3 and 8 ppm/°C. This design has 35 × 120 µm through glass vias (TGVs) and front and backside Cu routing metal. The routing metal and TGVs form electrically testable daisy chains. Samples of these glass interposers were subjected to 1000 thermal cycles from -40 °C to 125 °C to compare the two different glass compositions with regard to their long term reliability. Electrical testing on daisy-chained arrays of 400 TGVs each before and after thermal cycling showed no failures of the structures. In a separate test, Cu interdigitated test structures with 10 µm lines/space were fabricated on glass substrates of the same two types, on silicon with a thermal oxide layer, and also on fused silica. The leakage current between isolated structures was tested before and after 96 hrs of biased highly accelerated stress testing (HAST). The results indicate that for the glass substrate with a CTE of 8 ppm/°C, a barrier layer is necessary between the substrate and Cu metallization to prevent Cu migration.

Introduction

The advantages of highly engineered glass as a substrate material for microelectronics have been widely reported [1-4]. As the industry continuously pushes packages to higher signal frequencies and smaller line-widths, glass provides a low loss substrate with good dimensional control. Years of development in the display industry have resulted in a mature infrastructure for high volume glass forming processes, which can form glass substrates at design thickness as well as in panel format and will result in lower cost by leveraging economies of scale. The extensive development of glass substrates has also resulted in an advanced capability to engineer the thermomechanical properties of glass. One application that has garnered a lot of interest is for the use of glass for interposers, in which the ability to adjust the coefficient of thermal expansion (CTE) of glass can be leveraged to control warpage and improve reliability of bonded stacks comprised of different CTE materials [4]. For example, the CTE of the glass interposer could be matched to that of Si (3 ppm/C) or could be halfway between Si and a laminate substrate such as FR-4 (13 ppm/°C).

In addition to the technical advantages provided by the material properties of glass, there are significant opportunities to also positively impact the cost of fabricating glass interposers by leveraging high quality glass forming techniques to provide economies of scale (panel formation) as well as forming glass with thickness as low as 100 um thereby reducing or edeliminating process costs. This, as well as substantial advancements in the fabrication of blind and through holes in glass have been reported over the past few years. [5,6]

Modification of the CTE of glass substrates is accomplished by adjusting the composition of the glass, so there is great interest in understanding how glass composition may affect the electrical and reliability performance under different conditions. A few groups have reported on the electromigration of Cu redistribution lines (RDL) on glass of different types [7] and on the use of a barrier layer to prevent the diffusion of mobile alkali ions into thin film transistors fabricated on soda-lime glass [8]. Demir *et al.* has reported on the reliability through thermal cycling of un-filled Cu through glass vias (TGVs) in two polymer laminated glass types with CTEs of 3 and 8 ppm/°C and on the biased HAST testing of unfilled TGVs in the low CTE glass [9] and on thermal cycling of TGVs in bare glass [10].

Here, we report on two important aspects of the reliability of engineered glass and how the reliability of glass interposer structures is affected by changing glass composition. First, we study the reliability of fully-filled Cu TGVs during thermal cycle testing which may be affected by the changing CTE mismatch between copper and the different glass substrates. The test vehicle design is based on a thin, bare glass interposer with 35 µm x 120 µm fully Cu filled TGVs. Second, we study the reliability of voltage bias stressed Cu lines on glass during HAST testing which relates to the modification of the chemical composition of the glass and its compatibility with Cu metalization. In both cases, the glass substrates used were SGW3 and SGW8 substrates from Corning, Inc. with CTEs of 3 and 8 ppm/°C, respectively [6].

Thermal Cycle Testing

The fabrication of thin glass interposers with Cu filled through glass vias (TGV) was done using standard back end of line (BEOL) fabrication tools with no significant modification of any of the equipment wafer handling to accommodate glass wafers. In order to test the effect of the glass CTE on the long term reliability of the glass interposers, 150 mm glass wafers formulated with two different CTEs, 3 ppm/°C and 8 ppm/°C, were used in the fabrication process.

Full thickness 150 mm glass wafers with 35 µm x 125 µm blind TGVs were sputtered with a thin adhesion layer of Ti and Cu. No barrier or additional dielectric layer were deposited in the TGVs before the metallization. Highly conformal copper seed layers were deposited using metal-

organic chemical vapor deposition (MOCVD), in preparation for TGV plating. The seed layers were nominally 0.75µm in thickness, which was uniform throughout the TGVs. Electroplating of Cu was used to fully fill the TGVs and the overburden was removed using chemical mechanical polishing (CMP). High resolution x-ray imaging was used to verify the void-free nature of the Cu fill in the TGVs. To form the TGV test structures, plated Cu routing layers were patterned on both sides of the thin wafers. These routing layers were electroplated on a sputtered Ti/Cu seed layer with no barrier covering the glass substrate. Thin wafer handling was done using 3M's Wafer Support System (WSS). More details on the fabrication of these glass interposer test vehicle wafers can be found in previously published work [5].

After fabrication was completed, wafers from each glass type were electrically tested for continuity of the daisy chain test structures. Electrical continuity testing was done on eight test arrays, randomly chosen across the diameter of four wafers. Each test array consisted of 20 x 20 TGVs on 100 µm pitch, with each of the TGVs connected in series. The TGV test chain array, an example of which is shown in Figure 1, has testing points at the front and back of every TGV, so that any electrical discontinuity can be tracked down to the single metal link or TGV. The results of the initial round of electrical continuity testing are shown in Table 1. The combined yield of the TGVs and routing metal links was over 99.85% for both types of glass.

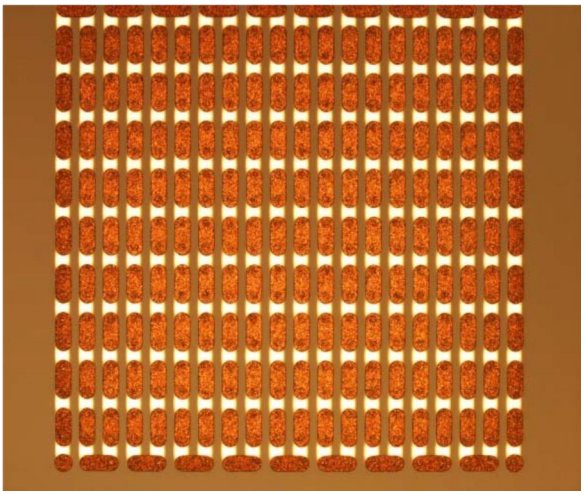

Figure 1. Optical microscope image of a TGV daisy chain test feature consisting of a 20 x 20 array of TGVs on 100 µm pitch. The topside metal links appear as copper colored and the links on the backside appear white.

Table 1. The results of 2-wire electrical continuity tests on 20 x 20 arrays of TGVs on 100 µm pitch

Wafer	CTE (ppm/°C)	No. of 20x20 arrays tested	Yield of TGVs & routing metal (%)
SGW3 - Wafer 1	3.2	8	99.97
SGW3 - Wafer 2	3.2	8	99.97
SGW8 - Wafer 1	8.1	8	99.72
SGW8 - Wafer 2	8.1	8	100.00

After this initial test, eight additional test arrays were selected from each type of glass with starting TGV array yields of 100%. These arrays were then subjected to thermal cycle testing, which consisted of 1000 cycles from -40°C to 125 °C with 1 hour cycle time and 15 min soak time at each temperature extreme (JEDEC JESD22-A104 condition G). An intermediate test point of 500 cycles was also done. The results of electrical testing at 0, 500 cycles, and 1000 cycles are shown in Table 2.

Table 2. The results of 2-wire electrical continuity tests on eight known-good 20 x 20 arrays of TGVs on 100 µm pitch before and after thermal cycle testing

No. of thermal cycles	Wafer	CTE (ppm/°C)	Yield of TGVs & routing metal (%)	Median chain resistance (Ω)
0 cycles	SWG3-Wafer 1	3.2	100.00	10.4
	SWG8-Wafer 2	8.1	100.00	6.7
500 cycles	SWG3-Wafer 1	3.2	100.00	15.4
	SGW8-Wafer 2	8.1	100.00	13.5
1000 cycles	SGW3-Wafer 1	3.2	100.00	16.6
	SGW8-Wafer 2	8.1	100.00	15.9

An increase in the median chain resistance was seen after thermal cycling. This was attributed to the oxidation of the unpassivated copper after exposure to the ambient air condition of the thermal cycling chamber. The calculated resistance value for the test chain array is 6.3 Ω, with each TGV contributing 4.5 mΩ.

Cross section samples were prepared from TGV test chains fabricated on both SGW3 and SGW8 substrates after 1000 thermal cycles. These images are shown in Figures 2, 3 and 4. The Cu filling of the TGVs had previously been verified to be void free by x-ray imaging, but no voids in the

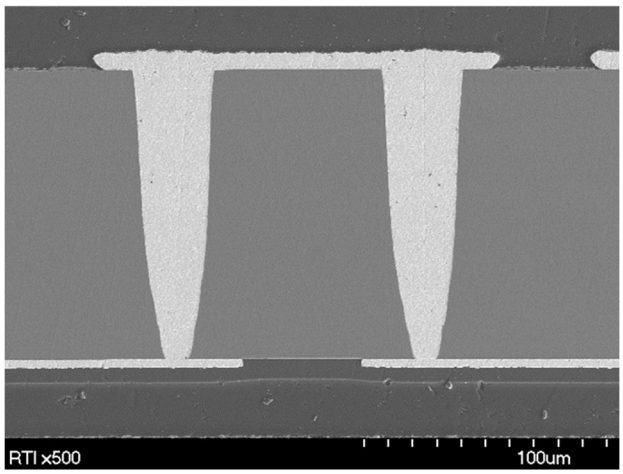

Figure 2. Cross section SEM image from an interposer test vehicle in SGW3 glass after 1000 thermal cycles. The angle of the cross section makes the TGVs appear more tapered than actual dimensions, which were measured to be from 17 µm to 19 µm in diameter at the wafer backside and 35 um diameter at the frontside.

TGVs or cracks in the glass around the TGVs were seen in either SGW3 or SGW8 samples after completion of the thermal cycle reliability tests. The tops and bottoms of the TGVs appeared to remain in stable contact with the Cu routing metal despite the lack of a stress buffer layer at either surface. While a more detailed elemental analysis technique is needed to determine whether Cu migration into the glass occurred during thermal cycling, no changes in the appearance of glass or Cu were seen by SEM around the Cu/Ti/glass interfaces.

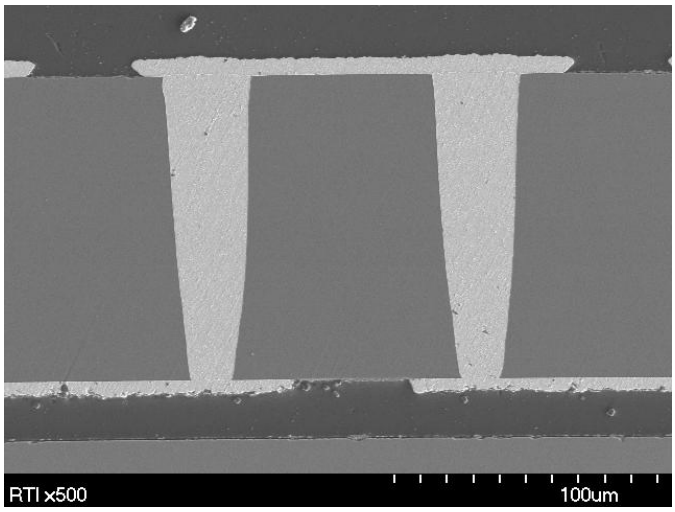

Figure 3. Cross section SEM image of an interposer test vehicle in SGW8 glass after 1000 thermal cycles. The TGVs were measured to be 35 µm in diameter at the top and 16 µm to 18 µm at the bottom.

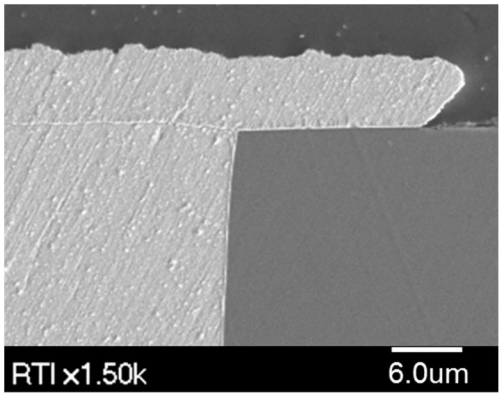

Figure 4. Cross section SEM image highlighting the TGV-to-top metal routing layer interface on an SGW8 substrate. No separation of this interface or cracking in the glass at the corner was seen after 1000 thermal cycles on either SGW3 or SGW8 substrates.

HAST Testing

In order to investigate the compatibility and reliability of Cu interconnections, whether these are routing metal layers or TGVs, with glass substrates of differing chemical properties, Cu test structures on different glass substrates were subjected to biased HAST reliability testing.

Test structures consisting of interdigitated Cu lines were fabricated on 100 mm glass wafers of differing composition and on silicon control wafers. These test structures were utilized for biased HAST testing experiments. Each wafer had six test sites, with each site having 400 fingers on 10 µm line/space and a 9 mm overlap of the fingers from each electrode. Table 3 lists the different substrates chosen for the HAST experiments. The silicon wafers were thermally oxidized with 3 kÅ of silicon dioxide. Some of the SGW8 glass wafers were coated with 1 µm of silicon nitride, which acts as a barrier layer to the alkali ions in this type of glass [2]. The silicon nitride was deposited at 200 °C using silane plasma enhanced chemical vapor deposition (PECVD). The SGW3 glass and fused silica wafers were not passivated with silicon nitride. To fabricate the interdigitated fingers a seed metal of 1000 A Ti and 1500 A of Cu was first deposited by sputtering. Lithography was used to pattern a resist template and copper was electroplated from a methanesulphonic acid (MSA) based bath from Enthone, Inc. After plating and photoresist strip, the seed metal was removed by wet chemical etching. To passivate the copper and protect it from outside contamination, a 5 µm thick coating of benzocyclobutene (BCB) 4024-40 from Dow was patterned over the fingers, leaving openings for the contact pads. While BCB is known to have low moisture uptake, it will allow moisture to pass through to the surface of the substrate. A solderable finish of NiAu was electroplated over the openings in the BCB for electrical connections to the electrodes.

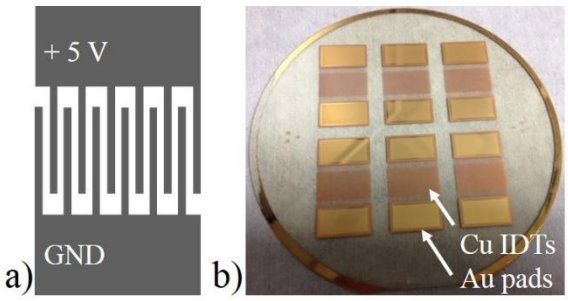

Figure 5. Interdigitated test structures shown in a) diagram form and b) on a 100 mm glass wafer

Table 3. A list of the different glass and silicon substrates with Cu IDTs chosen for biased HAST

Substrate types for HAST
SGW3
SGW8
SGW8 with 1 µm PECVD Si_3N_4
Fused silica
Si / 3kÅ thermal SiO_2

After fabrication was completed, leakage current measurements were taken at each test site using an IV sweep from -5 V to + 5 V using an Agilent 4155c parameter analyzer. The current measurement resolution of the testing station was measured to be about 15 pA. The leakage current measurements on the unpassivated SGW8 wafers were consistently higher than the other four substrate types.

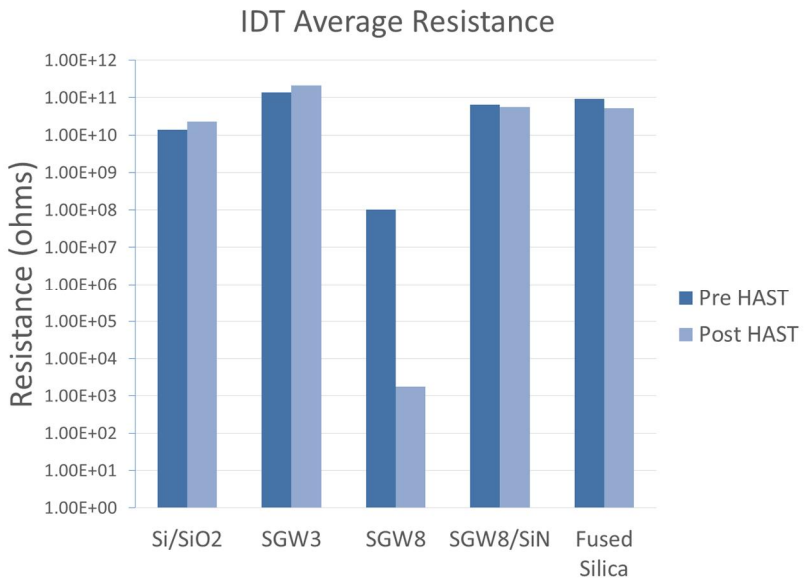

Figure 6. Graph of measured average resistance across Cu IDT structures fabricated on silicon and glass substrates of different compositions, before and after 96 hours of biased HAST testing.

The conditions of the HAST test chamber during testing were 130°C and 85% RH for a period of 96 hrs, using JESD22-A110-B. A 5 V DC bias was applied across the test site electrodes during testing. At least one IDT site on each wafer was left unbiased to decouple the effects of the high humidity/high temperature environment from the combined effects of voltage bias stress plus the high humidity/high temperature. These unbiased sites were not included in the leakage current averages recorded before or after HAST.

After HAST testing, the wafers were again electrically tested for leakage current across the interdigitated fingers using the same test conditions. Figure 6 shows a summary chart of the average electrical resistance measured from each substrate type before and after 96 hrs of biased HAST. The results before and after testing are largely unchanged for the silicon control wafers, the fused silica, the SGW3 glass, and the SGW8 glass with a Si_3N_4 barrier layer. However, a large decrease in resistance was observed on all IDTs on the SGW8 wafers without the barrier layer. Optical microscope inspection of the test sites on the unpassivated SGW8 glass wafers that had been under 5 V bias revealed a white substance between the fingers of the test features. Test sites from the same substrate which had not been under bias did not exhibit this appearance. None of the other substrates exhibited this change in appearance after HAST. Sample images taken from the four different glass substrates are shown in Figure 7.

To determine the chemical composition of the substance seen on the SGW8 glass with no barrier layer, samples from each wafer type were cleaved perpendicular to the Cu lines, imaged using scanning electron microscopy (SEM) and chemically analyzed using energy-dispersive X-ray spectroscopy (EDS). Because the samples were prepared by cleaving, the Cu lines appear pulled away from the surrounding BCB dielectric due to the ductility of Cu. SEM images from SGW3 are shown in Figure 8. On this substrate type, no difference in the glass composition was detected between the bulk substrate material and the area near the Cu lines or along the BCB/glass interface between the fingers. Specifically, no Cu was observed between neighboring Cu lines.

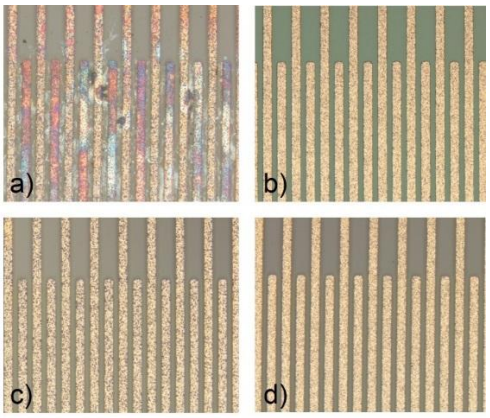

Figure 7. Optical microscope pictures taken after biased HAST testing of 10 µm line/space Cu IDTs on a) SGW8 glass, b) SGW8 glass with a Si_3N_4 barrier layer, c) SGW3 glass, and d) fused silica.

However, on the SGW8 substrate, EDS detected the presence of Cu in the white substance that could be seen from optical microscope inspection of the spaces between the Cu routing lines. Figure 9 shows two SEM images taken from an SGW8 sample without a nitride barrier. An EDS spectrum taken from the glass near the areas of Cu contamination indicated some migration of Cu not just along the interface, but into the glass. This can also be seen by the slight change in the color and appearance of the glass near the Cu particles. Similar analysis of the IDTs on SGW8 substrates with a Si_3N_4 barrier layer between the glass and the Cu lines, images from which are shown in Figure 10, shows no indication of Cu migration between the Cu fingers of the IDTs. These SEM and EDS observations were in agreement with the

measurements of leakage current, indicating that Cu migration was likely responsible for the leakage paths between the IDT fingers on the SGW8 substrates without a Si_3N_4 barrier layer.

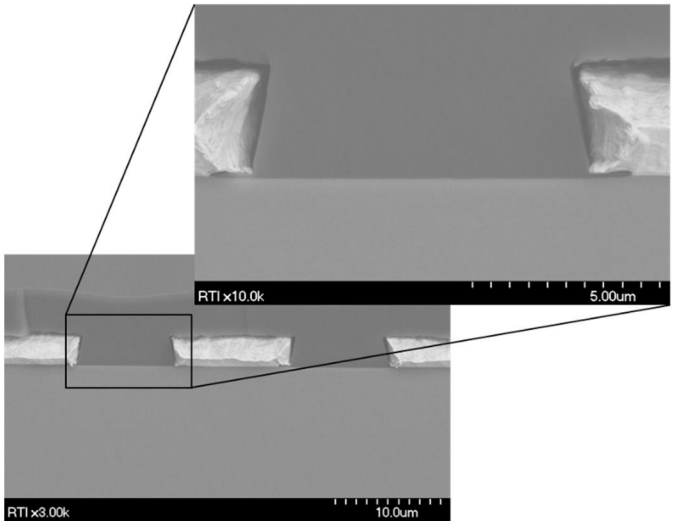

Figure 8. SEM images taken from a cleaved Cu IDT on an SGW3 substrate after biased HAST. No contamination was seen along the BCB/glass interface between the fingers.

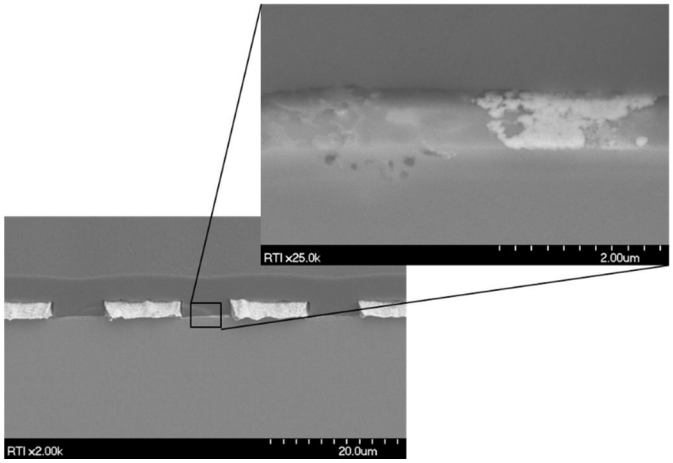

Figure 9. SEM images taken from a cleaved Cu IDT on an SGW8 substrate without a SiN barrier after biased HAST. Cu contamination was detected along the BCB/glass interface between the fingers.

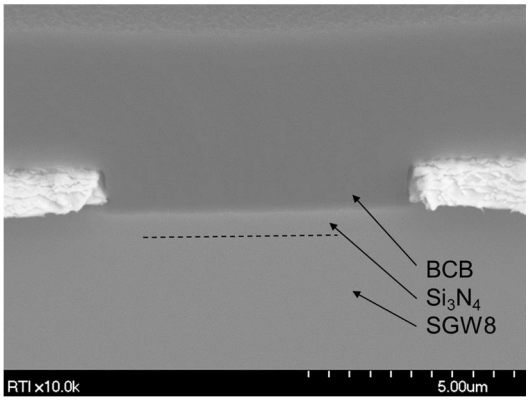

Figure 10. SEM images taken from a cleaved Cu IDT on an SGW8 substrate with a 1 µm SiN barrier after biased HAST. No Cu was detected by EDS analysis along the BCB/glass interface between the fingers.

Conclusions

Biased HAST and thermal cycling were used to examine two important aspects of the reliability of engineered glass as used in an interposer application. First, the reliability of Cu filled TGVs in SGW3 and SGW8 substrates was shown through 1000 thermal cycles from -40 – 125 °C. Test structures with 20 x 20 arrays of 35 µm x 120 µm TGVs arranged in serial daisy chain fashion were tested for electrical continuity and resistance before and after thermal cycling. All TGV arrays tested on both substrates were continuous after thermal cycling and no failures of TGVs or routing metal were observed. Cross section samples were prepared from the TGV arrays on both substrate types and imaged by SEM. Despite the mismatch in CTE between Cu and the glass substrates, no cracking of the glass or lifting of the routing was observed in the vicinity of the TGVs.

In the second part of the reliability testing, biased HAST was used to investigate the compatibility of Cu routing metal with glass substrates of different types. Cu IDTs with 10 um line/space were fabricated on SGW3, SGW8, SGW8 with 1 µm of Si_3N_4, fused silica, and Si with 3kÅ thermal oxide. Leakage current measurements taken across the IDTs before and after 96 hrs of biased HAST testing revealed a large drop in resistance only for the SGW8 substrate without a barrier layer. No significant change in the leakage current was seen on the other substrates after HAST, including SGW3 glass. Optical inspection combined with SEM/EDS analysis was used to determine that Cu migration along top surface of the SGW8 glass substrate was responsible for the leakage path. The Si_3N_4 layer provides an effective barrier against the mechanism causing the Cu migration. A barrier layer should be used between Cu metalization, whether in surface routing metal or as a TGV, and glass substrates engineered for high CTE.

Acknowledgments

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