Performance and Process Comparison between Glass and Si Interposer for 3D-IC Integration

Chun-Hsien Chien[1], Ching-Kuan Lee[1], Hsun Yu[1],Chang-Chih Liu[1], Peng-Shu Chen[1], Heng-Chieh Chien[1], Jen-Hau Cheng[1] , Li-Ling Liao[1], Ming-Ji Dai[1], Yu-Min Lin[1], Chau-Jie Zhan[1], Cheng-Ta Ko[1], Wei-Chung Lo[1], Lu, Yung Jean (Rachel)[2]

[1]Electronics and Optoelectronics Research Laboratories (EOL), Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan

[2]Corning Incorporated

[#]Tel: 886-3-5917854, Fax: 886-3-5917357, Email: ch_chien@itri.org.tw

Abstract

Nowadays, silicon is a mature material in semiconductor technology, but glass, a dielectric material, provides an attractive option due to its intrinsic characteristics for the advantages of electrical isolation, better RF performance, better feasibility with CTE and most importantly low cost solution. In this investigation, the glass interposer by using TSV industry equipment and tooling was evaluated and developed, and has been compared in complete processes and electrical/thermal characteristics with silicon interposer. In order to simulate and measure the electrical/thermal performance, patterned interposer wafer with 30μm diameter and 100μm depth Cu-filled TSVs are designed and prepared in advance. Key technologies include via fabrication, topside RDL formation, micro-bumping, temporary bonding, silicon and glass thinning and backside RDL formation were well developed and integrated to perform for comparison. 30μm via, 60μm pitch, RDL line/space 20μm/30um, 100μm thin wafer/glass and 15um micro-bumping been successfully integrated in the integration platform. The glass interposer was characterized and assessed to have excellent electrical performance and is potentially to be applied for 3D product applications.

Key words

TGV(Through-Glass Via), glass interposer, TSV(Through- Silicon Via), Silicon interposer, 3DIC, SiP

Introduction

There are lots of papers published and demonstrated for the Si interposer with 2.5D or 3D stacking integration due to its CTE matches to Si ICs, the wide availability of silicon infrastructure including the foundry wafer processes and the support of the Si equipments. Silicon interposer is also a good solution for high-pin-count ICs application based on the mature Si technology of advance via formation and fine line Cu damascene multilevel interconnection processes. However, silicon interposers suffer several issues compared with glass interposer; (1). Si material is semiconductor not good conductor or insulator, (2). Large difference of CTE exists between Cu and Si in TSV formation process, (3). Higher cost due to the need of electrical insulation around the via sidewall, (4). The limitation in size based on silicon industry. Therefore, it is very important to lower down the cost for mass production and one consensus on the cost of ownership is “the thinner, the better”. In another words, the lower aspect ratio application like CMOS Image Sensor of wafer level process is a good example.[1-4]

The main advantages of glass interposer including the inherent electrical property as an isolator, excellent insertion loss in high frequency RF application, better feasibility with CTE and large size availability for low cost solution. However, one of challenges is its lower thermal conductivity compared with silicon. Thermal conductivity of substrate used in 3D-IC is important for the overall thermal performance when multi chips are stacked on it. One of the key issues affecting performance is chip-to-chip thermal coupling on the substrate. The continued chip scaling has pushed the feature size of adjacent chips much closer, resulting in chip-to-chip thermal coupling. It is a challenge to decrease coupling effect due to small feature dimension. One promising solution is to use the low-thermal-conductivity substrate, such as, glass. Because of very low thermal conductivity of glass, the equivalent thermal conductivities, k_{xy} and k_z, of a through glass via (TGV) interposer are both much lower than those of a through silicon via (TSV) interposer structure. Simulation work for thermal characteristic of glass interposer has been studied extensively in Ref. [5]. The complete comparison study of the electrical design/simulation/measurement analysis, thermal performance, Si and glass interposer fabrication and characterization of the wafer-level integration scheme will be presented in the paper.

II. Structure design and Process Integration

A. The structures of Glass & Silicon interposers

The same masks were used on the processes of glass and

silicon interposers. So, identical transmission lines were both fabricated on glass and silicon interposers, as shown in Fig. 1.

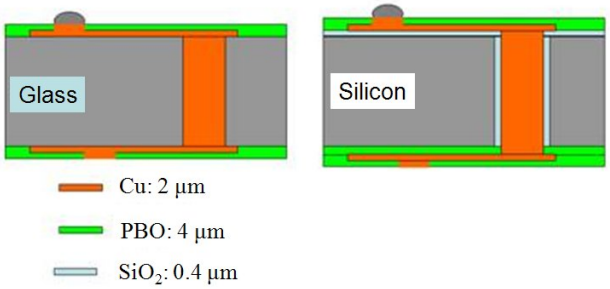


Fig. 1, the structures of glass & silicon interposer

An interposer includes a substrate and two metal layers which were disposed on the opposite sides of the substrate. The substrate was glass or silicon. The structures of transmission lines include micro-strip, CPW and CPWG + 2 Vias. In a micro-strip structure, the signal line and the ground plane were disposed on the opposite sides of the substrate, as shown in Fig. 2. In a CPW (coplanar waveguide) structure, the signal and ground were both disposed on the same side of the substrate, as shown in Fig.3. Another transmission line combined two through vias (TGVs or TSVs) and a CPWG (coplanar waveguide with ground), which constituted a transition of the signal line through the substrate, as shown in Fig. 4. As a result, the design rule of glass and silicon interposers was generalized by analyzing the characteristics of transmission lines by measurement and simulation.

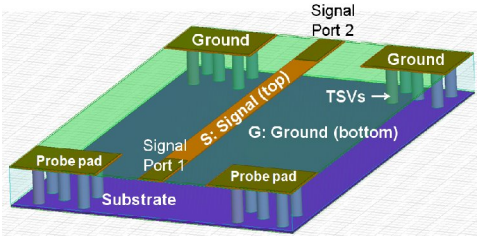


Fig. 2, the structure of micro-strip with line width 70 μ m

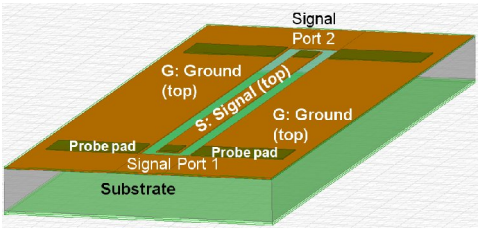


Fig. 3, the structure of CPW with line width 54μm and gaps 30μm between the signal line and the surrounded ground plane

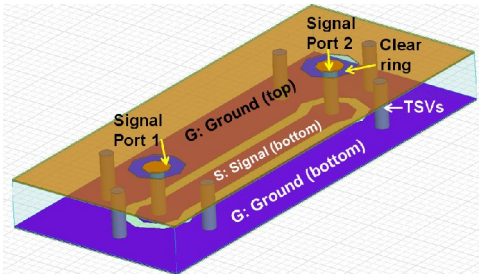


Fig. 4, the structure of CPWG + 2 Vias with line width 70μm and gaps 30μm between the signal line and the surrounded ground plane

B. Process Integration

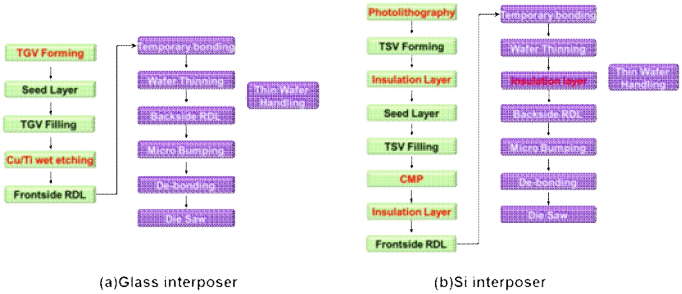


Fig. 5 process flow for interposer: a)Glass interposer, b)Si interposer

-Glass interposer

The process flow for manufacturing TGV/RDL interposer is displayed in Figure 5a. The interposer (100μm) is fabricated on a 300mm Glass substrate. TGV is formed directly on glass wafer by Corning. After Ti barrier and Cu seed-layer process, Cu plating with a bottom-up mechanism is applied to minimum the overburden on the wafer surface. Cu overburden and Ti barrier are removed by wet etching process. For top RDL (line-width = 20μm), Cu plating process with seed layer (Ti/Cu) wet-etching process is applied. The PBO material is used for passivation, the process temperature is blow 200°C. Top UBM (15μm in diameter; 4μm/5μm-thick Cu/Sn) is formed with a top passivation opening (15μm). Wafer thinning starts with the temporary bonding with a carrier at the front-side (glue thickness = 20μm). Grinding/CMP is used for the Cu revealing. Bottom RDL is then formed by Cu plating after lithography patterning. Bottom UBM (85~120μm in diameter) is formed with a PBO passivation opening of 85~120μm.

-Si interposer

The process flow compared with Glass interposer is shown in Fig 5b. The flow in detail is also described as below. The interposer (100μm) is fabricated on a 300mm P-type Si (100) substrate. After deposition of inter-layer dielectrics (to isolation Si substrate and subsequent top RDL), TSV is

etched by dry etching with BOSCH-type process to form a vertical sidewall. TSV SiO_2 liner is formed by SACVD to ensure a high step-coverage along the TSV sidewall. After Ta barrier and Cu seed-layer process, Cu plating with a bottom-up mechanism is applied to minimum the overburden on the wafer surface. Cu overburden and Ta barrier are removed by CMP process. For top RDL, passivation process, UBM formation, thin wafer handling, Cu revealing are same to Glass interposer flow. Then the backside isolation is also applied with PBO material (highest process temperature is 200℃). Bottom RDL, passivation, bottom UBM formation are also same to Glass interposer process.

III. The Electrical Evaluation of Glass & Silicon Interposer

C. Assessing Silicon conductivity

Silicon conductivity could be assessed by a micro-strip line through measurement and simulation. The supplier provided silicon resistivity as 14.07 ~ 20.75 OHM*CM [8], i.e. conductivity 4.82 ~ 7.1 Siemens/meter.

First, the micro-strip was measured twice with insertion loss being 1.0 dB. Then, the micro-strip was simulated by ANSYS HFSS [7] with the parameters listed in Table I. It could be found that the conductivity introduced the insertion loss in a variation of 1.7 dB to 2.4 dB at 10 GHz, as shown in Fig. 6. While the insertion loss was measured at 1.0 dB, the silicon conductivity of 3 Siemens/meter was determined thereafter.

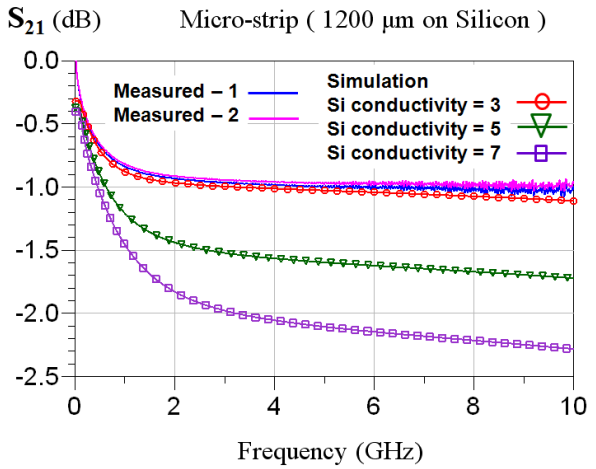


Fig. 6, the insertion loss of a micro-strip with length 1200µm on Silicon interposer, comparing the measured with simulation of the variation of silicon conductivity 3~7

D. Micro-strip & CPW Lines

In order to compare electrical properties of glass and silicon, we analyzed transmission lines (Tr-lines) of identical dimensions, which were fabricated on glass and silicon interposers.

The design parameters of micro-strip and CPW transmission lines were tabulated in Table II. Then, the characteristic impedance Zc and insertion loss S_{21} were simulated through [7] & [9], as shown in Fig. 8 & 9. Fig. 9 shows that Tr-lines on glass got much less insertion loss than those on silicon. Fig. 9 also showed that the simulation agrees with measurement at 0.1 to 10 GHz.

Furthermore, the relations of line width and characteristic impedance Zc were generalized in Fig. 7, with reference to Fig. 8 and Table II. Comparing with identical line width, Tr-lines on glass got higher impedance Zc than those on silicon. The Zc of Tr-lines on silicon rose with frequency and approached 50Ω at higher frequencies. Because the port impedances were set 50Ω for measurement and simulations, the Zc of Tr-lines should approach 50Ω for less insertion loss. Generally, Zc should be designed in the range of 45 ~ 55Ω. Tr-lines on glass apparently did not lie in this range. In the next section, Tr-lines were further designed to approach 50Ω by simulation tools.

Table I, the material properties for simulation

Material	Relative Permittivity	Loss Tangent	Conductivity
Glass	5.013 ~ 5.129	0.0046 ~ 0.00586	0
PBO	3.5	0.02	0
SiO2	4	0.001	0
Silicon	11.9	0	3 ~ 7 Siemens/meter

Table II, the design parameters of transmission lines

		Micro-strip	CPW
Line Width (µm)	Glass	70	54
	Silicon	70	54
Line Length (µm)	Glass	1200	1200
	Silicon	1200	1200
Gap (µm)	Glass	115	30
	Silicon	115	30
Height (µm)	Glass	101	101
	Silicon	95	95
Zc (Ω)	Glass	78.7 ~ 83.1	62.4 ~ 76.3
	Silicon	14.0 ~ 53.1	14.0 ~ 47.2

***** Note: Gap is the distance between signal pad and ground pad. Height is the thickness of glass or silicon substrate.

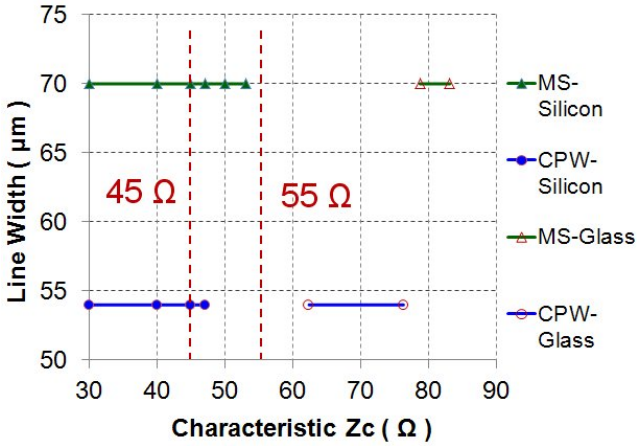


Fig. 7, the design parameters of Tr-Lines on Glass & Silicon interposers

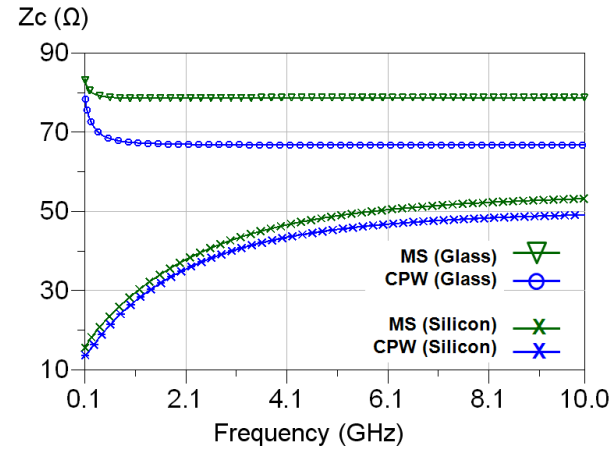


Fig. 8, the characteristic impedance Zc of Tr-Lines on Glass & Silicon interposers, verified by simulation

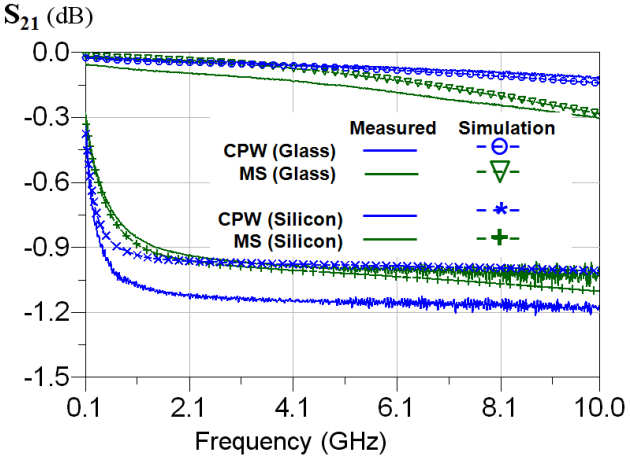


Fig. 9, the insertion loss S_{21} (dB) of Tr-Lines on Glass & Silicon interposers, verified by measurement and simulation

E. Transmission Lines with Impedance 50Ω

The gaps and line width were adjusted to make characteristic impedance Zc approaching 50Ω through simulations, as shown in Fig. 11. Therefore, Tr-lines have different dimensions in Table III and Fig. 10. Tr-lines on glass had larger line width compared to those on silicon. Fig. 10 showed that the structure 'CPWG + 2Vias' had minimum line width for Tr-lines approaching 50Ω. Furthermore, CPWG + 2Vias also had minimum insertion loss both on glass and silicon interposers, as shown in Fig. 12. So, 'CPWG + 2Vias' had compact size for 50Ω along with better performances.

Besides, Tr-lines with largest line width had worst performances. For example, CPW on glass had largest line width 272 µm along with critical Gap 22 µm. In Fig. 12, CPW had worst insertion loss among Tr-lines on glass.

Table III, Design Parameters of Tr-Lines approaching 50Ω

Glass (G) and Silicon (Si)		Micro-strip	CPW	CPWG	CPWG + 2Vias
Line Width (µm)	G	168	272	74	74
	Si	80	50	40	40
Line Length (µm)	G	1200	1200	1200	1200
	Si	1200	1200	1200	1200
Gap (µm)	G	66	22	30	30
	Si	110	32	30	30
Height (µm)	G	101	101	101	101
	Si	95	95	95	95
Zc (Ω)	G	50 ~ 55	51 ~ 62	42 ~ 50	52 ~ 60
	Si	14 ~ 52	14 ~ 48	30 ~ 48	20 ~ 51

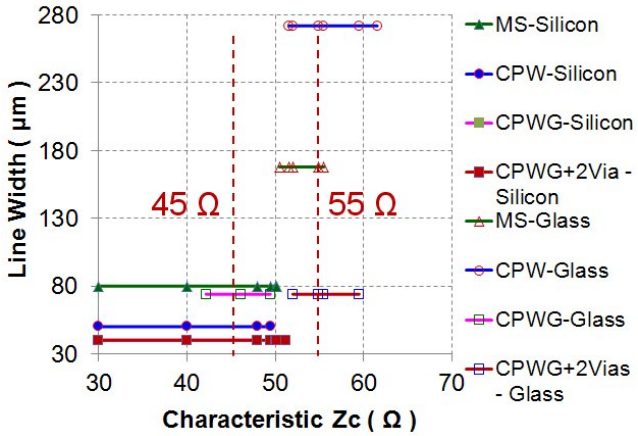


Fig. 10, the design parameters of Tr-Lines on Glass & Silicon interposers, whose characteristic impedance Zc approaching 50Ω

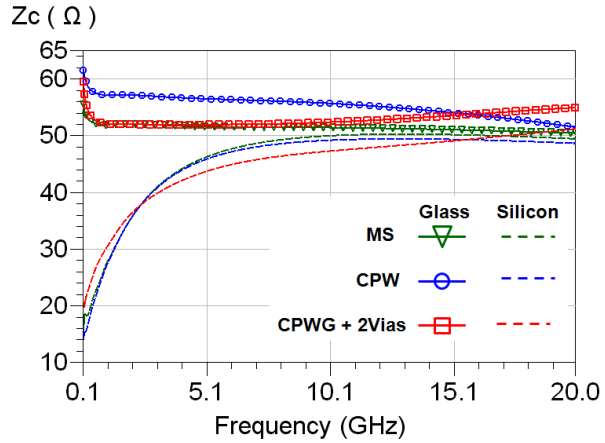


Fig. 11, the characteristic impedance Zc of Tr-Lines on Glass & Silicon interposers, verified by simulation

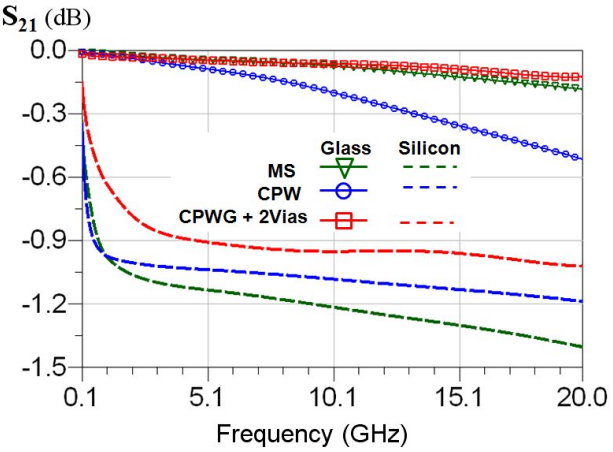


Fig. 12, the insertion loss S_{21} (dB) of Tr-Lines on Glass & Silicon interposers, verified by simulation

IV. Thermal Performance Comparison

We have successfully fabricated a glass and silicon interposers, as shown in Fig.13, to study the thermal coupling effect. Two interposers were fabricated by the processing flow described in the previous section. The schematic drawing of the experimental setup to measure temperature distribution of interposer under power loading is shown in Fig.14. Both interposers were respectively placed on a thermoelectric (TE) device with three copper blocks as dummy chips. The TE device, functioned as a heater, can quickly heat the interposer through copper blocks to a specified power condition uniformly. We recorded the temperature profiles of interposers at the same power input into TE device in order to compare the heat spreading between glass and silicon.

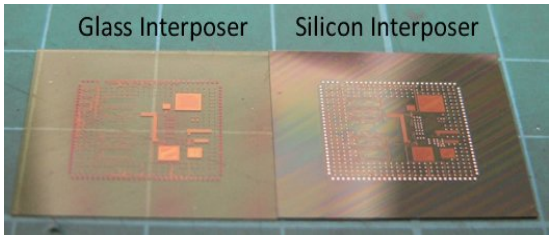


Fig.13: Photo image of glass and silicon interposers. Glass (left) and silicon (right) interposers were constructed in the same pattern design of copper via/trace.

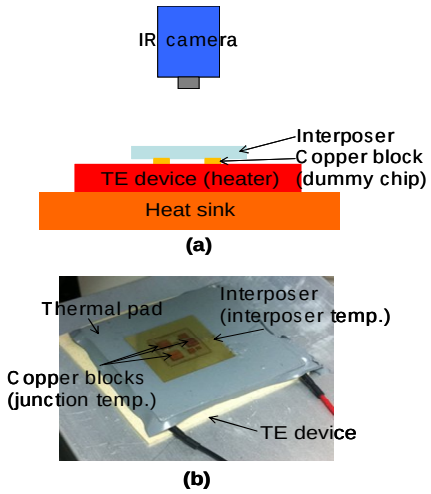
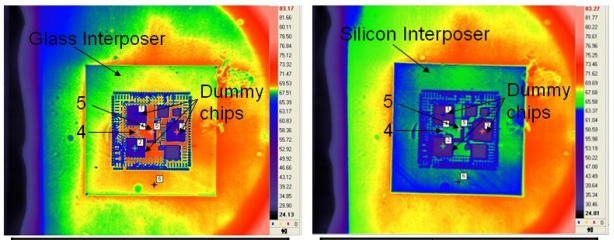


Fig.14: Schematic drawing (a) (not to scale) and photo image (b) of experimental setup for temperature distribution measurement. Both interposers were tested under the same heating condition supplied by TE device through cooper blocks.

The temperature profiles of glass and silicon interposers under the same heating condition are shown in Fig.15. It is clear that junction temperatures (points 1~3) of copper blocks measured from the glass interposer are higher than those from silicon interposer. Heat could not be effectively spread out to the surrounding area in the glass interposer so localized high temperature at heating location is apparent. The temperatures measured between dummy chips (copper blocks) from glass interposer (point 4~5) are very close to those from silicon one. Due to the low thermal conductivity in in-plane direction (k_{xy}) of glass, the temperatures between dummy chips placed on the glass interposer were not influenced with each other thermally. Glass interposer is sufficient to avoid the thermal coupling/cross-talk among chips not only single-chip but also multi-chips stacking in 3D-IC integration.



Measurement Point	Temperature (C)	Emissivity
1	104.24	0.22
2	104.78	0.22
3	105.55	0.22
4	71.97	0.94
5	70.99	0.94

Temperature Point	Temperature (C)	Emissivity
1	77.52	0.22
2	77.39	0.22
3	74.49	0.22
4	70.38	0.80
5	70.67	0.80

(a) (b)

Fig. 15: (a) Thermal profile of glass interposer under thermal loading. The temperatures at point 4 and 5 are 71.97 and 70.99 degree C, respectively. The emissivity in IR camera was corrected for corresponding materials in the experiment. (b) Thermal profile of silicon interposer under the same thermal loading as glass interposer. The temperatures at point 4 and 5 (70.38 and 70.67 degree C, respectively) are very close to those of glass interposer.

V. Glass Interposer Assembly

Once the interposer was fabricated, the daisy-chain designed chip was assembled on the interposer by chip-to-chip (C2C) bonding. Before bonding process, both the surfaces of test chip and silicon/glass interposer were pretreated by Ar/H_2 plasma to remove the oxidation layer upon micro bumps for joining. The bonding condition of 250°C/5sec was selected while the bonding pressure of 8N was adopted to ensure the connectivity of micro joints. After chip bonding process, capillary-type underfill was used to fill the gap between chip and interposer. Figs. 16(a) and 16(b) show the chip-stack modules of silicon and glass interposers, respectively. Fig. 17 displays the cross-sectioned microstructure of micro joints within the silicon and glass interposer module. From the magnification images of micro joints in Figs. 17(a) and 17(b), the connectivity of micro joints was confirmed and the solder within the micro joints was mostly transformed into IMC. The gap between chip and interposer was less than 10μm and fully filled by underfill, as seen in Fig. 17. It should be noted that delamination shown in the figure was caused by grinding and polishing during sample preparation for SEM observation. Even delamination was occurred within the SEM sample, however the micro joints was joined very well.

The resistance of daisy chain (804 I/Os) is around 65.24ohm and bump resistance of Kelvin structure is around 34 mohm ~ 44 mohm after TEG chip bonding on glass interposer which the measurement results meet our expectation.

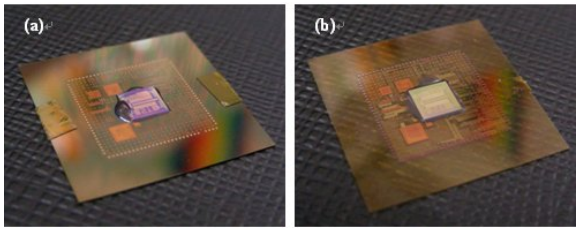


Fig.16 (a) Si interposer module and (b) glass interposer module.

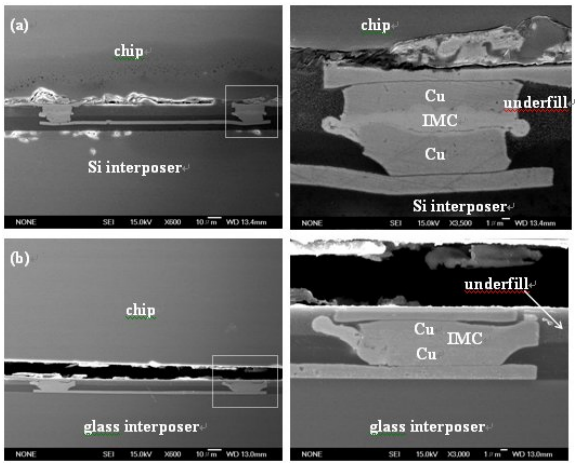


Fig.17 Cross-sectioned microstructure of micro joints within (a) Si interposer module and (b) glass interposer module.

VI. Conclusion

A wafer-level 300mm glass interposer scheme with topside RDL, Cu TGVs, bottom side RDL, Cu/Sn micro-bump and PBO passivation has been successfully developed and demonstrated in the study.

The characteristics of transmission lines are investigated both on glass and silicon interposers. The silicon conductivity could be assessed by comparing the simulation and measurement of micro-strip. Besides, the design rule of Tr-lines was generalized by a chart of line width versus characteristic impedance Zc. From this chart, it can be concluded that the structure of 'CPWG + 2Vias' has minimum line width for 50Ω. This structure also has better performances among Tr-lines on glass and silicon interposers.

As for the thermal performance, glass interposer is sufficient to avoid the thermal coupling/cross-talk among chips not only single- but also multi-chip stacking in 3D-IC integration. Besides, we had successfully developed a fabrication and assembly process for glass interposer. the characterization results indicate that the 3D integration scheme possesses excellent electrical performance, and could be extensively applied for 3D product applications.

Acknowledgment

This research is supported by the ITRI-Corning

collaboration project and the Ministry of Economic Affairs(MOEA), Taiwan, ROC. Authors greatly thank to the Ad-STAC members, AMAT, SUSS, DISCO, and Brewer Science for the experiment assistance.

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